

**REMARKS**

This responds to the Office Action dated on November 21, 2006.

No claims were amended, added, or cancelled herein. Claims 1-17 are pending.

**§102 Rejection of the Claims**

Claims 1-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Canella Jr. et al. (U.S. Patent No. 6,144,561, hereinafter “Canella”).

Canella describes a reconfigurable connectorization panel assembly for a circuit board housing rack. A motherboard installed in the housing rack receives circuit modules. Each circuit module includes a motherboard connector and can include one or more plug action connectors. The plug action connectors are configured to extend through an opening in the motherboard and an opening in the back of the housing rack. A connectorization panel associated with each circuit module is bolted to the back of the housing rack such that a corresponding plug-action connector mates with the connector extending out the rear of the housing rack. The connectorization panel therefore adapts a particular slot in the housing rack for a particular type of input/output cabling and connectors.

In contrast, Applicant teaches, and claims in claims 1-17, a system which uses a replacement module to connect two or more circuit boards attached to an embedded backplane. If two circuit boards required higher data transfer bandwidth, the replacement module can be swapped out for one which enables the desired data transfer bandwidth.

The Examiner stated that Canella discloses a daughter board (circuit module 18) and two or more replacement modules (connectorization panels 15a-15h). Even if this were true, the Examiner has failed to show where Canella discloses:

a replaceable module positioned proximate to the embedded backplane and adapted to receive the daughter boards, the replaceable module includes one or more data paths, wherein each data path transfers data between two or more daughter boards;

wherein the embedded backplane and the replaceable module are configured such that data transfer bandwidth can be added between the two or more daughter boards without replacing the embedded backplane.

as required by claims 1-12. There is no circuit module to circuit module communication shown in Canella. Even if there was, there is no teaching or suggestion to use the connectorization panels to enhance circuit module to circuit module communication.

Furthermore, Applicant teaches, and claims in claims 11 and 12, that the replaceable module operates in conjunction with a router board to distribute signals from the router board to one or more daughter (circuit) boards, and from one or more daughter (circuit) boards to the router board. Canella has no such teaching.

Likewise, the Examiner has failed to show where each connectorization panel includes:

a plurality of connections in communication with the data paths for connecting at least one of the data paths to two or more printed circuit boards such that one of the printed circuit boards can transfer data to another of the printed circuit boards across the data path;

as required by claims 13-17. Again, there is no circuit module to circuit module communication shown in Canella. Even if there was, there is no teaching or suggestion to use the connectorization panels to enhance circuit module to circuit module communication.

Applicant teaches, and claims in claims 13-17, that a replacement module also includes alignments means for positioning the module with respect to the backplane. The alignment means is configured such that data transfer bandwidth can be added between the two or more daughter boards plugged into the embedded backplane without replacing the embedded backplane.

alignments means for positioning the module with respect to the backplane, wherein the alignment means is configured such that data transfer bandwidth can be added between the two or more daughter boards plugged into the embedded backplane without replacing the embedded backplane.

Furthermore, Applicant teaches, and claims in claims 15-17, that the replacement operates in conjunction with a router board to distribute signals from the router board to one or more daughter (circuit) boards, and from one or more daughter (circuit) boards to the router board. Canella has no such teaching.

Reconsideration of claims 1-17 is respectfully requested.

**CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

**Reservation of Rights**

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of

**RESPONSE UNDER 37 CFR § 1.116 – EXPEDITED PROCEDURE**

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priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Respectfully submitted,

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By their Representatives,

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Date

January 22, 2007

By

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Date of Deposit: January 22, 2007 (Monday)

This paper or fee is being filed on the date indicated above using the USPTO's electronic filing system EFS-Web, and is addressed to: The Commissioner for Patents, MS AF, P.O. Box 1450, Alexandria, VA 22313-1450.

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